Appl. No. 09/972,576

IN THE CLAIMS

1. (Currently Amended) A semiconductor arrangement comprising:

[[•]] a substrate having a substrate layer ~~(13)~~ with an upper surface and a lower surface, the substrate layer ~~(13)~~ being of a first conductivity type;

[[•]] a first buried layer ~~(12)~~ in the substrate, extending along said lower surface below a first portion of said upper surface of said substrate layer ~~(13)~~, and a second buried layer ~~(12)~~ in the substrate, extending along said lower surface below a second portion of said upper surface of said substrate layer ~~(13)~~;

[[•]] a first diffusion region ~~(26)~~ in said first portion of said substrate layer ~~(13)~~, being of a second conductivity type opposite to said first conductivity type and having a greatest depth at a first point along a width of said first diffusion region ~~(26)~~ and having a lesser depth at a second point along said width; ~~and~~

[[•]] a shallow region ~~(27)~~ in said first portion of said substrate layer ~~(13)~~, being of said first conductivity type and being on top of said second point of said first diffusion region ~~(26)~~ but not on top of said first point of said first diffusion region ~~(26)~~;

[[•]] a second diffusion region ~~(45)~~ in said second portion of said substrate layer ~~(13)~~, being of said second conductivity type;

a first polysilicon structure, of the second conductivity type in contact with the first diffusion region;

a second polysilicon structure, of the first conductivity type, in contact with the shallow region; and

a dielectric spacer disposed between the first and second polysilicon structures.

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2. (Currently Amended) The arrangement according to claim 1, wherein said first diffusion region ~~(26)~~ is a base ~~(3)~~ of a bipolar transistor, said shallow region ~~(27)~~ is an emitter ~~(4)~~ of said bipolar transistor, and said first buried layer ~~(12)~~ is a collector ~~(5)~~ of said bipolar transistor.

3. (Currently Amended) The arrangement of according to claim 1, wherein said second diffusion region ~~(45)~~ is an anode of a protection diode ~~(9)~~ and said second buried layer ~~(12)~~ is a cathode of said protection diode ~~(9)~~.

4. (Currently Amended) The arrangement according to claim 1, wherein said first buried layer ~~(12)~~ is connected to said second buried layer ~~(12)~~, and said first and second buried layers ~~(12)~~ are manufactured in the same step.

5. (Currently Amended) The arrangement according to claim 1, further comprising a channel stopper region ~~(42)~~ in said second portion of said substrate layer ~~(13)~~; the channel stopper region ~~(42)~~ being of said first conductivity type, for electrically isolating said second portion of said substrate layer ~~(13)~~ within the substrate ~~(6)~~, wherein said channel stopper region ~~(42)~~ is arranged to extend substantially as an extended channel stopper region ~~(47)~~ in between said second diffusion region ~~(45)~~ and said second buried layer ~~(12)~~.

6. - 8. (Cancell d)

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9. (Currently Amended) A **The** semiconductor arrangement as recited in claim 3, wherein said protection diode is a pn junction diode.

10. (Currently Amended) A **The** semiconductor arrangement as recited in claim 1, further comprising a channel stopper between said second diffusion region ~~(45)~~ and said second buried layer.

11. (New) A semiconductor structure, comprising:

a substrate of a first conductivity type;

a first doped region disposed in the substrate, the first doped region of a second conductivity type;

an epitaxial layer disposed over the substrate and the first doped region, the epitaxial layer of the second conductivity type;

a first dielectric layer disposed over the epitaxial layer, the first dielectric layer having a plurality of opening therethrough;

a doped plug disposed in the epitaxial layer between a top surface of the epitaxial layer and a portion of the first doped region, the doped plug aligned with a first one of the plurality of openings in the first dielectric layer;

a first patterned doped polysilicon structure disposed over the first dielectric layer, and further disposed around an edge of a second one of the plurality of openings in the first dielectric layer, the first doped polysilicon structure of the first conductivity type;

a second dielectric layer disposed over the first dielectric lay r and the first pattern doped polysilicon structure, the second dielectric layer having a plurality of openings therethrough, a first one of the plurality of openings in the second dielectric layer being aligned with the first one of the openings in the first dielectric layer, and a second one of the plurality of openings in the second dielectric layer being aligned with the second one of the openings in the first dielectric layer;

a dielectric spacer disposed around an edge of the second one of the plurality of openings in the second dielectric layer;

a doped polysilicon plug disposed in through the second opening of the second dielectric layer, the doped polysilicon plug of the second conductivity type;

a second doped region of the second conductivity type disposed in the epitaxial layer at a surface portion of thereof and in contact with the doped polysilicon plug;

a third doped region of the first conductivity type disposed in the epitaxial layer subjacent the second doped region; and

a fourth doped region of the second conductivity type, disposed in the epitaxial layer, aligned with, and spaced apart from, the third doped region, the fourth doped region further spaced apart from the first doped region.

12. (New) The semiconductor structure of Claim 11, further comprising:

a second patterned doped polysilicon structure disposed over the first dielectric layer, and further disposed in a third one of the plurality of openings in the first dielectric layer, and in contact with the epitaxial layer, the second doped polysilicon structure of the first conductivity type; and

a fifth doped region of the first conductivity type, subjacent the second patt rned doped polysilicon structure, the fifth doped region in contact with the second patterned doped polysilicon structure.

13. (New) The semiconductor structure of Claim 12, further comprising a channel stopper region having a first portion disposed in the epitaxial layer, and a second, portion disposed in the substrate, the channel stopper region of the first conductivity type, the first and second portions contiguous with each other.

14. (New) The semiconductor structure of Claim 12, wherein the third doped region comprises a first portion having a first thickness; and a second portion having a second thickness; wherein the first and second thicknesses are different.

15. (New) The semiconductor structure of Claim 12, wherein the first conductivity type is p-type and the second conductivity type is n-type.

16. (New) The semiconductor structure of Claim 12, wherein the dielectric spacer comprises silicon nitride.

17. (New) The semiconductor structure of Claim 12, wherein the fifth doped region has a third thickness, and the third thickness is greater than the first thickness and greater than the second thickness.